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# MOSFETs ASM Integrated Circuit – DrMOS

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## Abstract

This paper discusses and demonstrates the performance of integrated MOSFET and driver products. In order to develop the devices, it was necessary to understand the requirements of the synchronous-buck circuit topology, optimize the silicon process to provide low switching and conduction losses, and develop packaging technology that provides compact and easy assembly. Experimental and simulation results show good performance for core voltage power supplies and point of load (POL) converters.

## Topology Design Concerns

In the synchronous-buck circuit (as shown in Figure 1), the key requirements that need to be understood are MOSFET optimization, switching losses, conduction losses, shoot-through ruggedness and gate-driver timing.

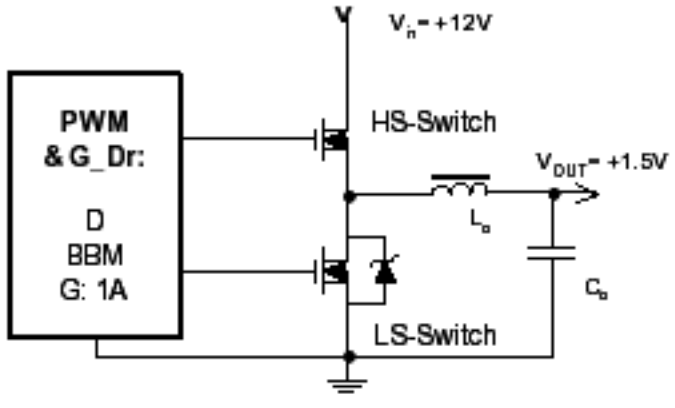


**Figure 1.** Synchronous-buck topology

MOSFET optimization depends upon the duty cycle of the high-side switch. For a notebook core application, the duty cycle can be less than 10% due to 18-V input and 1.6-V typical output. For desktop applications, the duty cycle can be around 13% with a 12-V input and 1.6-V output. For POL converters, the duty cycle can be 25% to 50% depending on the requirements. For the low duty cycle applications, the size of the high-side MOSFET is usually smaller than the low-side to minimize the switching losses. The low-side MOSFET size is optimized to minimize conduction losses. Figure 2 shows the analysis of how efficiency can vary for various die sizes (x-axis). For a fixed process technology and MOSFET cell density, desktop applications provide the best performance with a 1:2 die-size ratio. As the die size increases, switching losses start to dominate and reduce efficiency. As the die size decreases, conduction losses tend to drive efficiency lower.

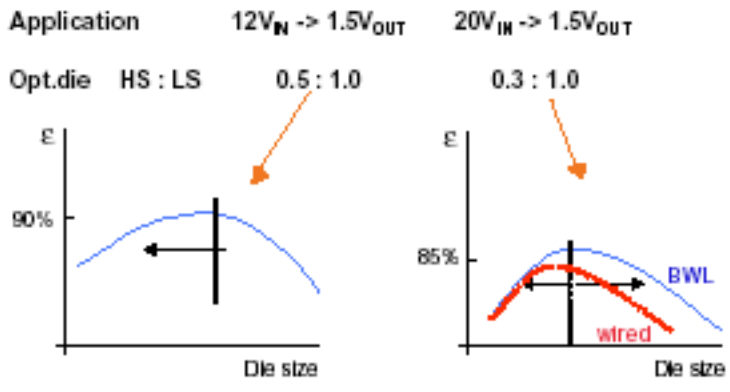


**Figure 2.** Die size optimization

Switching losses typically are controlled through adaptive switching, which ensures that the high-side is turned off before the low-side turns on, thereby reducing any shoot-through conditions. However, the low-side turn-off and high-side turn-on usually are fixed times. When this time is long, say 50 ns, there is the possibility that the low-side body diode will conduct and reduce the efficiency of the circuit (as shown in Figure 3). Reducing dead time can minimize this body diode conduction (Figure 4). Furthermore, the peak ringing

voltage also can be reduced and thus put less stress on the MOSFET, allowing designers to use a lower $V_{DS}$-rated MOSFET for improved performance or reduced cost.

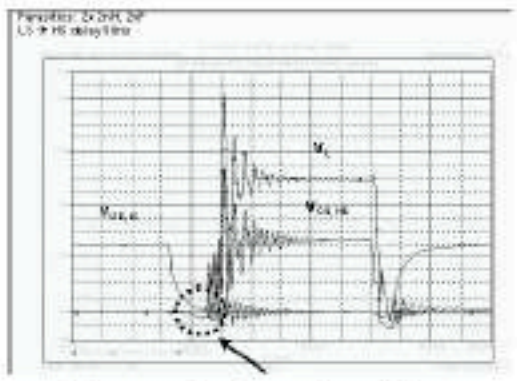

**Figure 3.** Long dead time

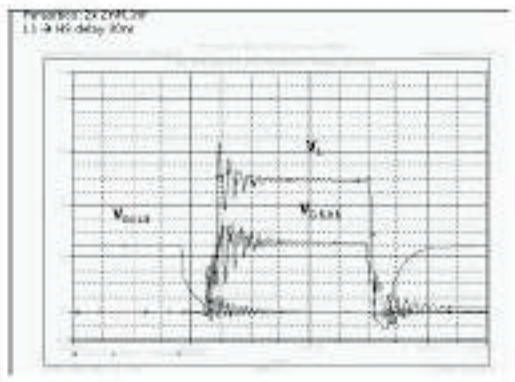

**Figure 4.** Short dead time

Using simulations with the 9 mm by 9 mm MLF MOSFET packaging (discussed later in this paper), efficiency can vary depending on the dead time selected for the driver. Figure 5 shows the simulation results. The goal is to optimize the dead time for best efficiency.

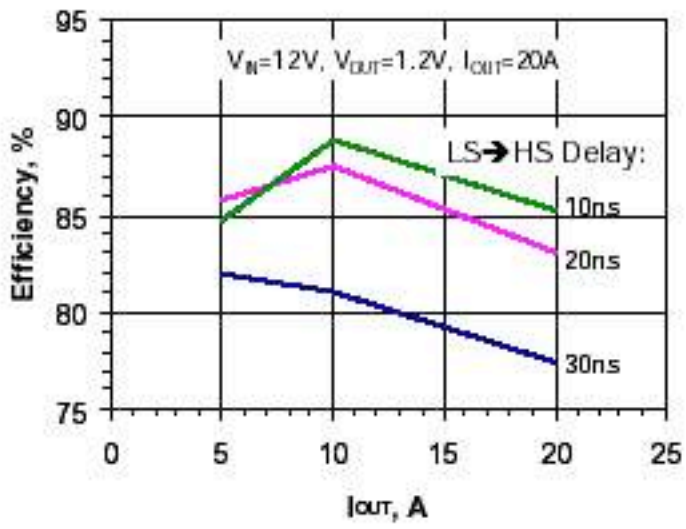


**Figure 5.** Efficiency by dead time

**Silicon Technology Advancement**

One silicon optimization method is to use a MOSFET with a lower gate threshold, $V_{th}$. This has three effects on the MOSFET (Table 1).

| Event | Issue | Parameters | Effects |
|---|---|---|---|
| Turn-off | Ringing | $t_f = R_G C_{iss} / Vth$ | Allows longer turn-off time |
| Turn-on | Body diode | $t_r = R_G C_{iss} / (V_{GS}-V_{TH})$ | Reduces rise time |
| Conduction | Low $R_{DS}$ | $R_{DS} \sim 1 / (V_{GS}-V_{th})$ | Lower R |

**Table 1.** Effects of low $V_{th}$

For the turn-off period, a lower $V_{th}$ slows down the turn-off and also allows some shoot-through to help dampen any ringing that is the result of the high-side turning on. A lower threshold helps in turning on the low-side MOSFET by reducing the rise time. This is more applicable with a 5-V gate drive. The third effect of the lower threshold is the reduction of conduction losses due to lower $R_{DS}$. This effect also is applicable with a 5-V gate drive.

Lowering the threshold of the MOSFET can be done in one of two ways: lowering the doping or thin the gate oxide. Lowering the doping requires a longer channel length to help maintain sufficient charge to prevent punch-through: $Q_{ch} = N_{dop} * L_{ch}$. Increasing the channel length increases the $C_{rss}$ and $R_{DS}$ of the MOSFET. Thinning the gate oxide will result in an increase in the capacitance, $C_{iss}$ and $C_{rss}$: $C_{gx} = e / T_{ox}$; thus, this can increase switching losses when used at frequencies above 300kHz. However, for low-frequency applications with low gate-drive voltage, say 300kHz and 5 V, a lower-gate-threshold device can offer better performance.

The final silicon optimization that is required is the optimization of shoot-through ruggedness. This occurs when the high-side turns on, causing a high dV/dt transistion of the switching node. The sharp voltage rise can inflict a voltage pulse on the low-side MOSFET gate due to the Miller capacitance (Figure 6). When lowering the gate threshold, this condition is more of a concern. However,

proper selection of MOSFET parameters and optimization of the MOSFET process can help reduce this effect. With control the ratio of the

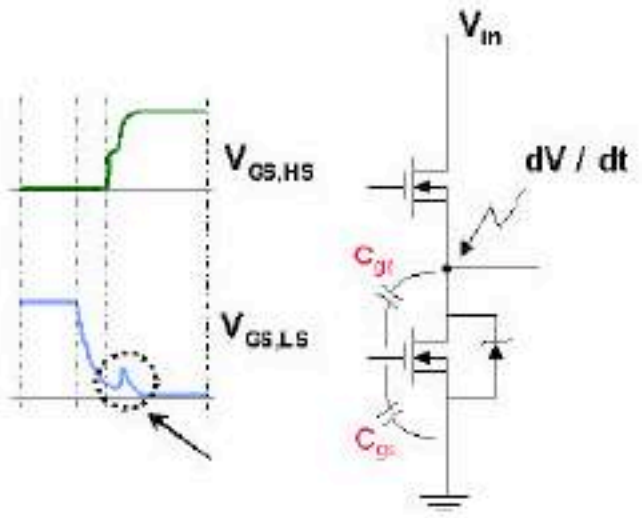


**Figure 6.** Shoot-through condition

Miller capacitances, $C_{gd}$ and $C_{gs}$, the $V_{GS}$ pulse may be limited by the equation

$$V_{GS}(t_0) = R_G * C_{rss} * \frac{V_{DS}}{t_o}\left(1 - e^{\frac{-t_0}{R_G * C_{iss}}}\right)$$

For a set condition, a family of curves can be generated (Figure 7). For a $C_{iss}$=4nF, the $C_{rss}/C_{iss}$ ratio needs to be less than 0.4 ($Q_{gd}/Q_{gs}$ ratio of 1.0) for a typical threshold of 1.8 V to 2 V. Use of a low-threshold MOSFET requires a ratio of less than 0.25 ($Q_{gd}/Q_{gs}$ ratio of 0.8).

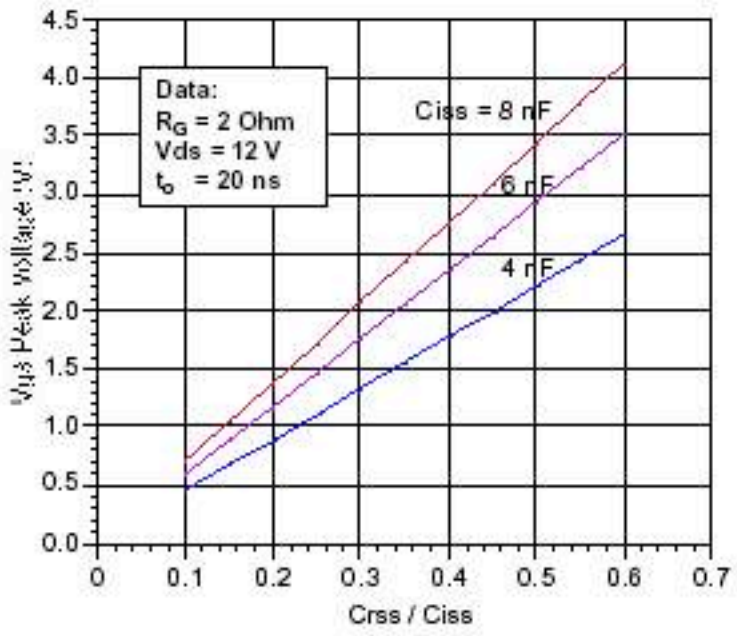


**Figure 7.** Shoot-through ruggedness

New MOSFET processing technologies have been developed to lower the MOSFET $R_{DS}$, reduce switching losses, and lower $Q_{GD}$. The first process improvement was to increase the cell density and reduce the trench depth. Increasing the density requires a narrower trench and thus a reduction in the $Q_{GD}$. The increased cell density also allows for more parallel trenches and a reduction in the MOSFET resistance per area. For comparison, previous MOSFET technology for an SO-8 package yielded an $R_{DS}$-$Q_G$ figure of merit of 240m? -nC, with a maximum $R_{DS}$ at 4.5 V and typical $Q_G$ at 4.5 V. The higher-cell-density $R_{DS}$-$Q_G$ figure of merit is 110m? -nC. A new MOSFET technology, called WFET has been developed to further lower the $Q_{gd}$ value of a MOSFET by using a thick-bottom oxide process (Figure 8). The WFET technology results in a narrower plateau for the $Q_G$ curve (Figure 9). This process can lower the $Q_{gd}$ (the plateau) by ½ when compared to the conventional process. The WFET process allows for faster switching for high-side applications by reducing the overall $Q_G$, and improves shoot-through immunity by lowering the $Q_{gd}/Q_{gs}$ ratio.

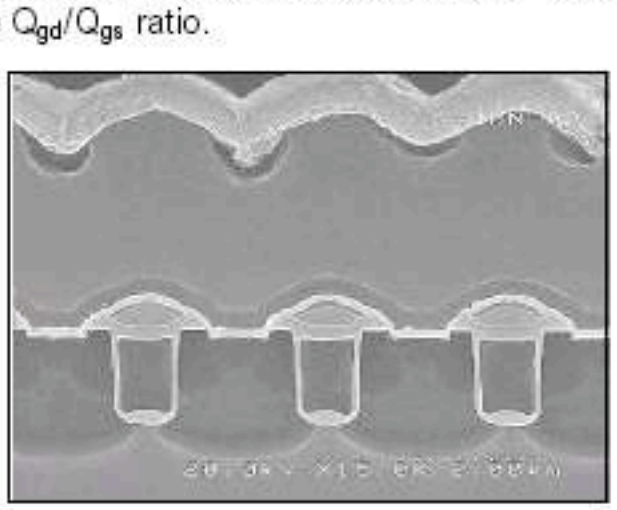

**Figure 8.** WFET cross-section

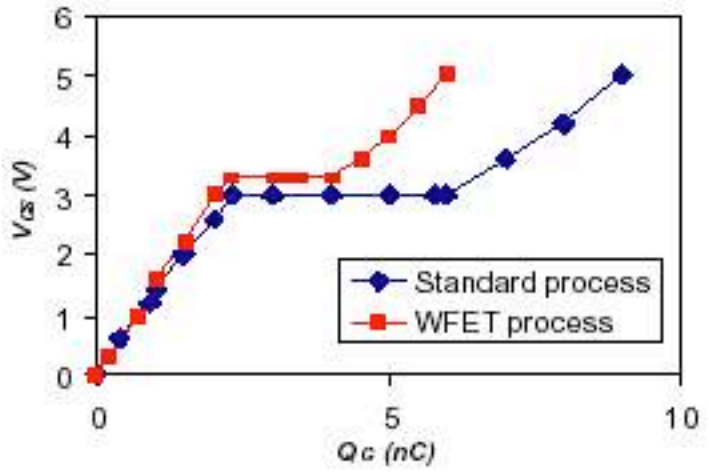


**Figure 9.** Improved Qg curve

## Package Technology

To prove out the MOSFET-driver product concept quickly, Vishay Siliconix developed an SO-16-packaged product. The development of new silicon technology and further understanding of the requirements has resulted in a family of SO-16 devices that include integration of a Schottky diode with the low-side MOSFET (Si4724CY) and two sets of MOSFET voltage ranges: 30 V (Si4768CY) and 20 V (Si4770CY). The 30-V products allow usage with applications such as notebook computers. The 20-V products are useful for desktop applications and POL converters, and they allow for better MOSFET parameters such as lower $R_{DS}$ and smaller switching losses. Figure 10 shows a set of 30-V products and illustrates the efficiency versus the application current.

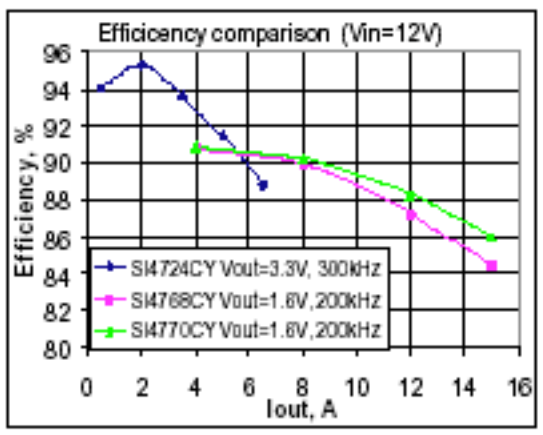


**Figure 10.** SO-16 product efficiency

The SO-16 product efficiencies tend to limit around 15 A for 200 kHz when used for computer-related applications. This limitation was based on a 4-phase evaluation board as shown in Figure 11.

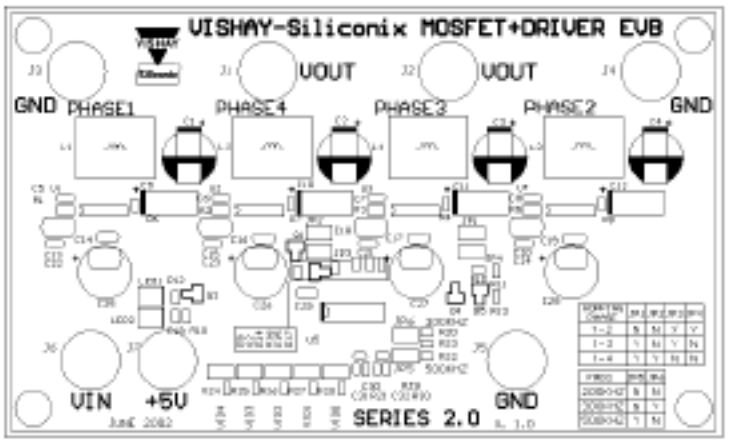


**Figure 11.** Four-phase SO-16 evaluation board

The next goal was to meet a 20-A, 1-MHz-per-phase capability. This required a move to a more thermally enhanced package while maintaining a small board area. Siliconix is developing a 9 mm by 9 mm MLF package that will achieve this target (Figure 12). By combining the optimization of the die size, dead time control, shoot-through immunity, and new silicon process technology, simulation show that an efficiency approaching 84% is possible. Furthermore, with the additional packaging development of using bond-wireless technology, significant efficiency improvement can be made through reduction of the package inductance. Figure 13 shows this step-wise efficiency improvement using simulations.

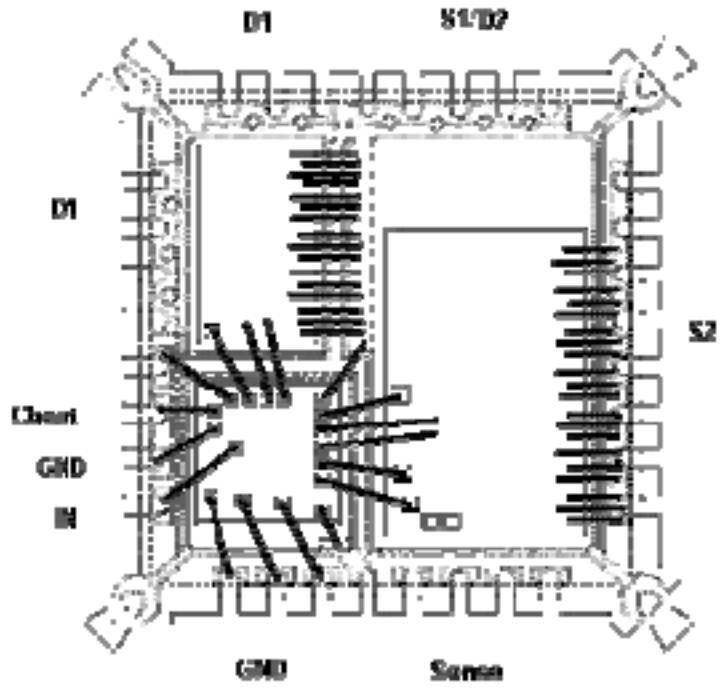


**Figure 12.** 9 mm by 9 mm MLF device

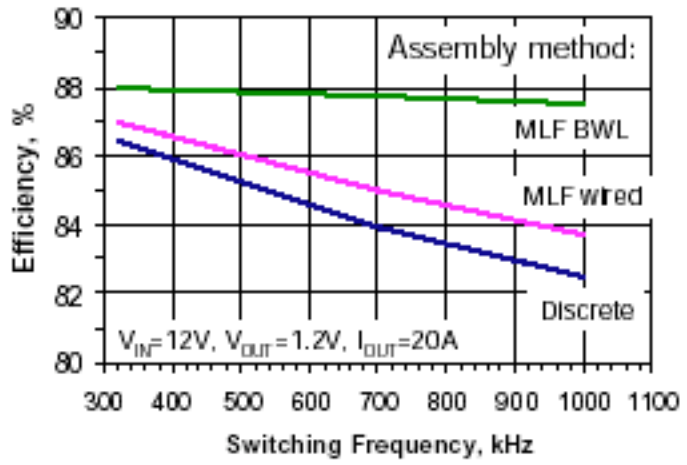


**Figure 13.** 9x9 MLF efficiency improvement

## Further Test Results

As stated earlier, the goal was to show efficiency results for computer core voltage power supplies and POL converters. Computer results have been shown already (Figure 5 and Figure 13). Because POL converters do not necessarily require the high current outputs, SO-16 devices were deemed to be adequate. Figure 14 shows the efficiency results for a set of POL conditions. Here, the efficiencies are above 85% for the SO-16 package (Si4768CY) with loads up to 14 A.

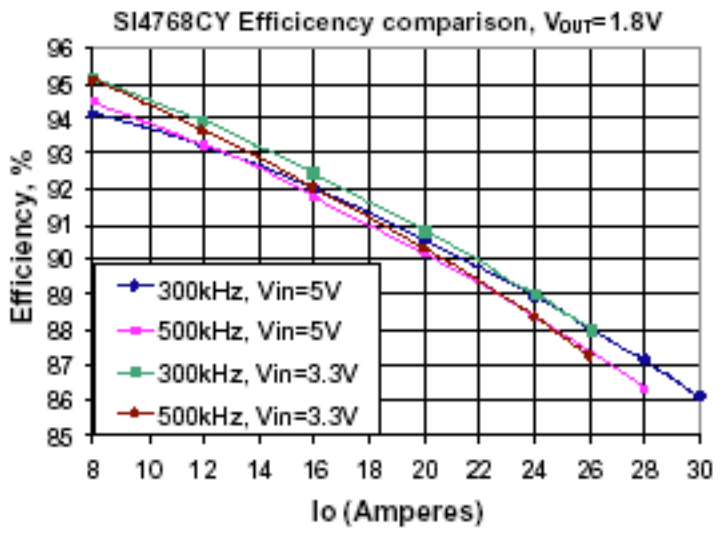


**Figure 14.** POL efficiency results

## Conclusions

Integrated MOSFET and driver products can bring a performance improvement for POL converters, as well as for computer core voltage and for other DC-to-DC synchronous-buck power supplies. Built on a clear understanding of the requirements of the circuit topology and optimization of both silicon and packaging, an integrated device can provide reduced space and better performance compared to a discrete solution.